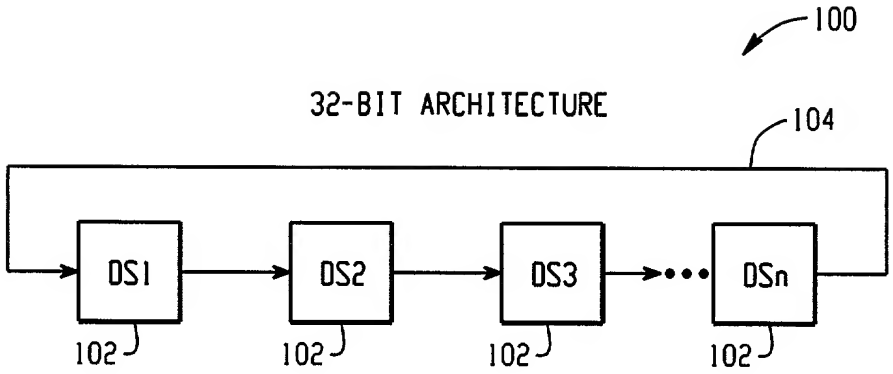
100
32-BIT ARCHITECTURE
104
DS1
DS2
DS3
DSn
102
102
102
102

Fig. 1

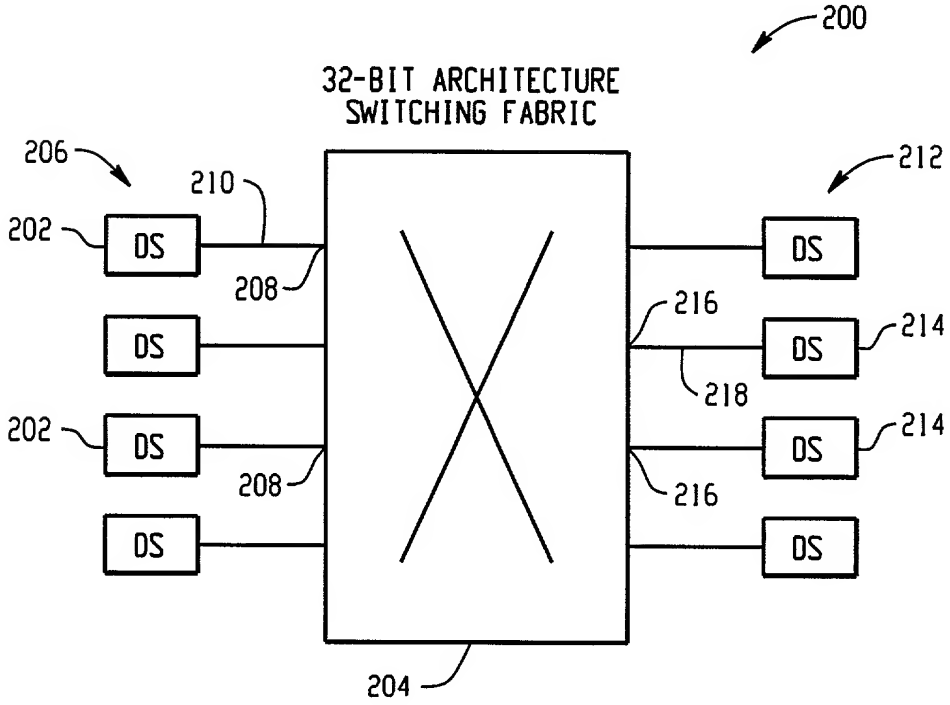
200
32-BIT ARCHITECTURE
SWITCHING FABRIC
206
210
212
202
DS
208
216
214
DS
218
202
DS
208
214
216
DS
DS
204

Fig. 2

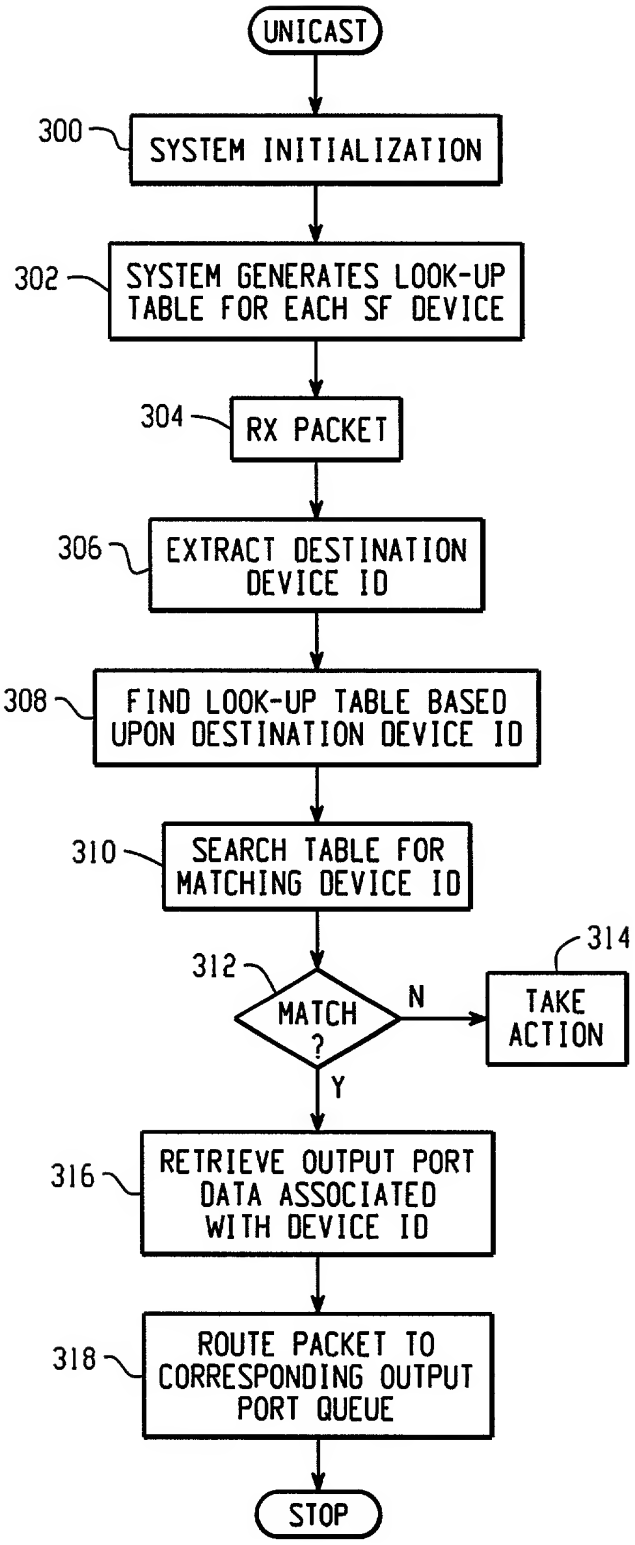

Fig. 3

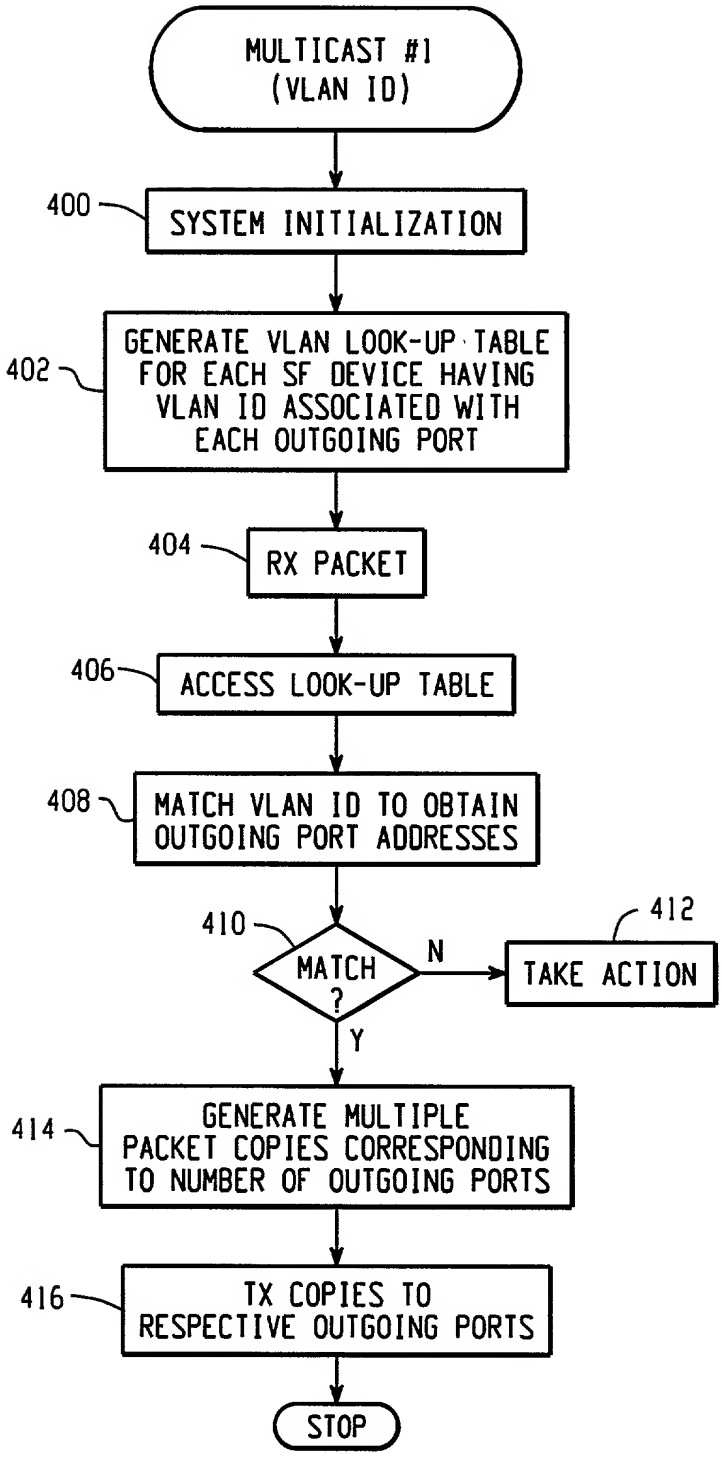

Fig. 4

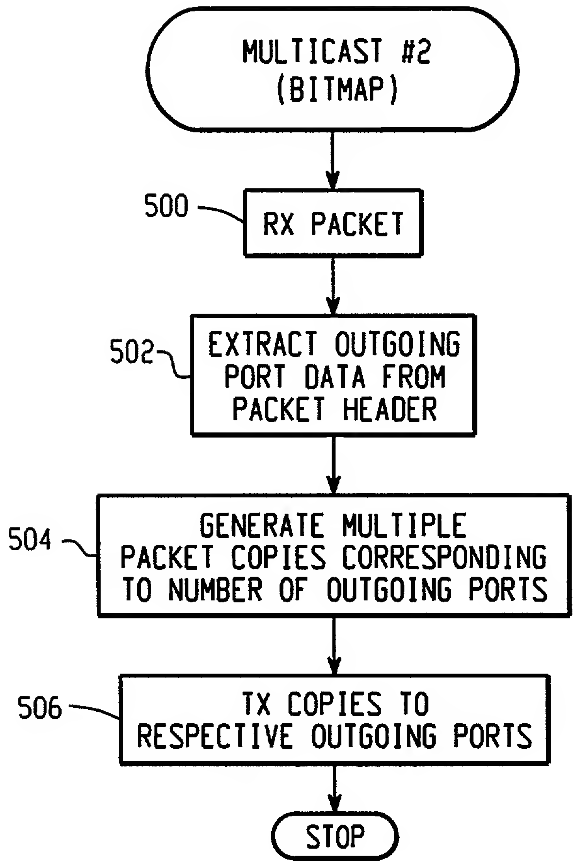
MULTICAST #2
(BITMAP)
500
RX PACKET
502
EXTRACT OUTGOING PORT DATA FROM PACKET HEADER
504
GENERATE MULTIPLE PACKET COPIES CORRESPONDING TO NUMBER OF OUTGOING PORTS
506
TX COPIES TO RESPECTIVE OUTGOING PORTS
STOP

Fig. 5

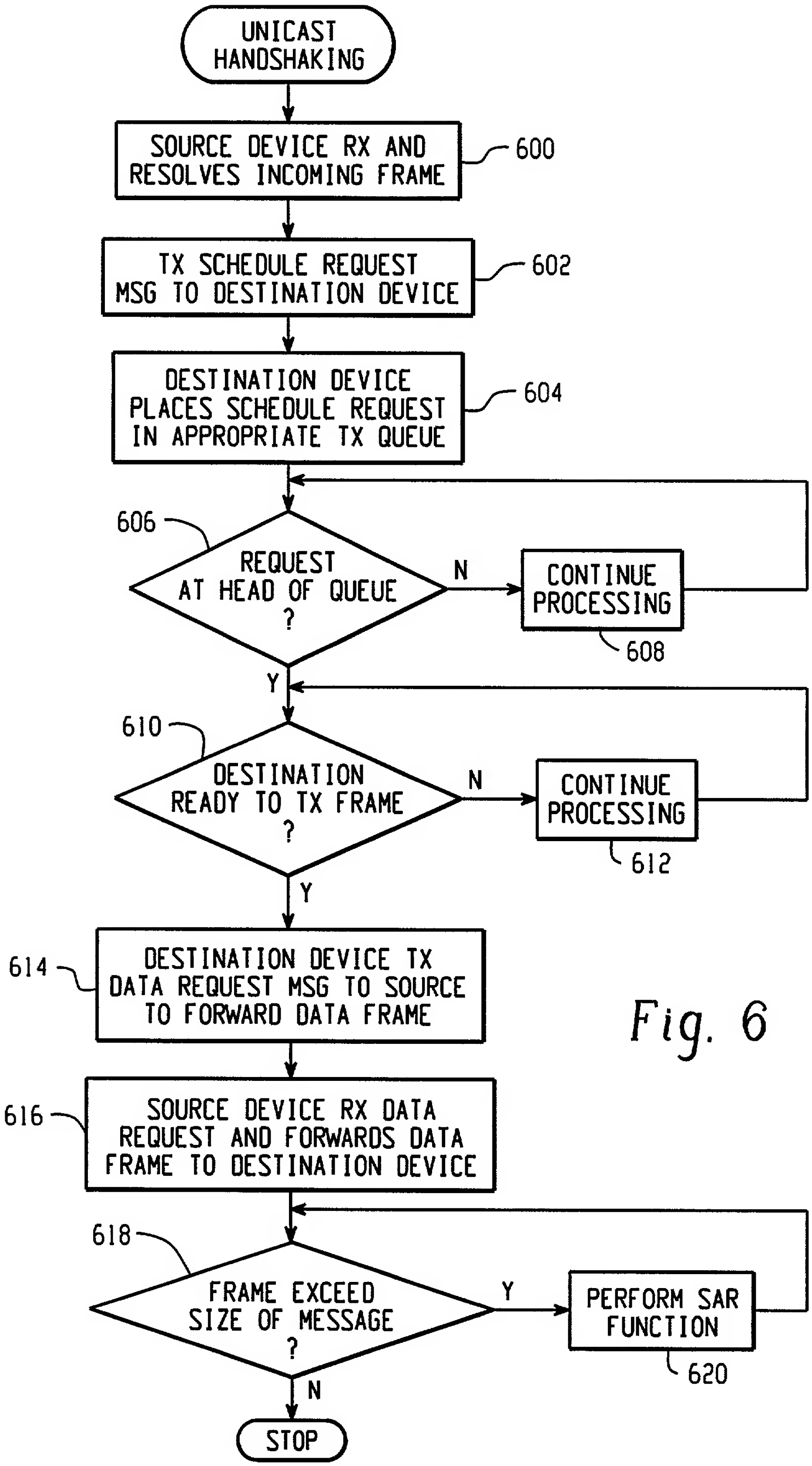
UNICAST HANDSHAKING
SOURCE DEVICE RX AND RESOLVES INCOMING FRAME
600
TX SCHEDULE REQUEST MSG TO DESTINATION DEVICE
602
DESTINATION DEVICE PLACES SCHEDULE REQUEST IN APPROPRIATE TX QUEUE
604
606
REQUEST AT HEAD OF QUEUE ?
N
CONTINUE PROCESSING
608
Y
610
DESTINATION READY TO TX FRAME ?
N
CONTINUE PROCESSING
612
Y
614
DESTINATION DEVICE TX DATA REQUEST MSG TO SOURCE TO FORWARD DATA FRAME
616
SOURCE DEVICE RX DATA REQUEST AND FORWARDS DATA FRAME TO DESTINATION DEVICE
618
FRAME EXCEED SIZE OF MESSAGE ?
Y
PERFORM SAR FUNCTION
620
N
STOP

Fig. 6

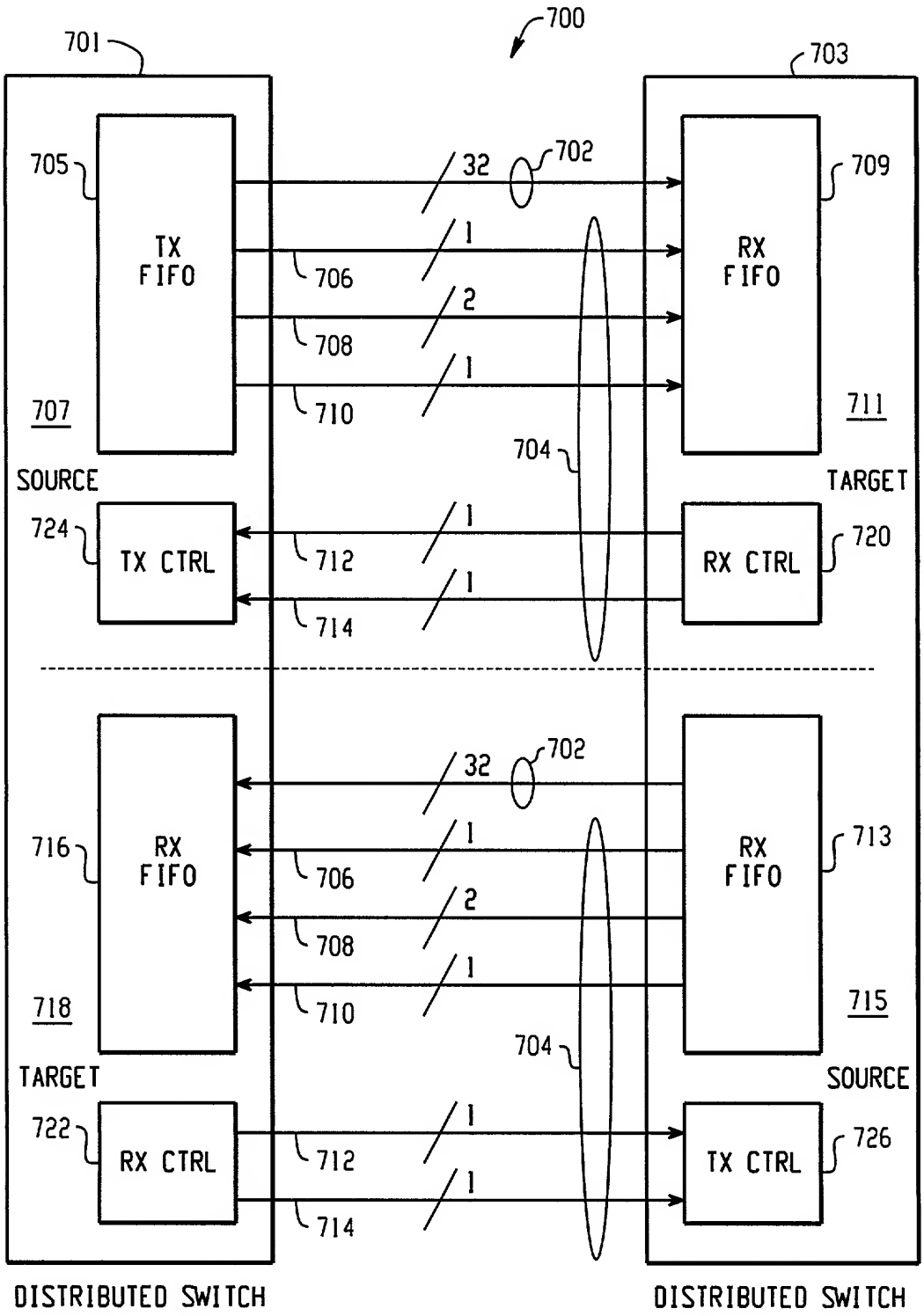
700
701
703
705
TX FIFO
32
702
709
RX FIFO
1
706
2
708
1
710
707
711
704
SOURCE
TARGET
724
TX CTRL
1
712
1
714
RX CTRL
720
716
RX FIFO
32
702
713
RX FIFO
1
706
2
708
1
710
718
715
704
TARGET
SOURCE
722
RX CTRL
1
712
1
714
TX CTRL
726
DISTRIBUTED SWITCH
DISTRIBUTED SWITCH

Fig. 7

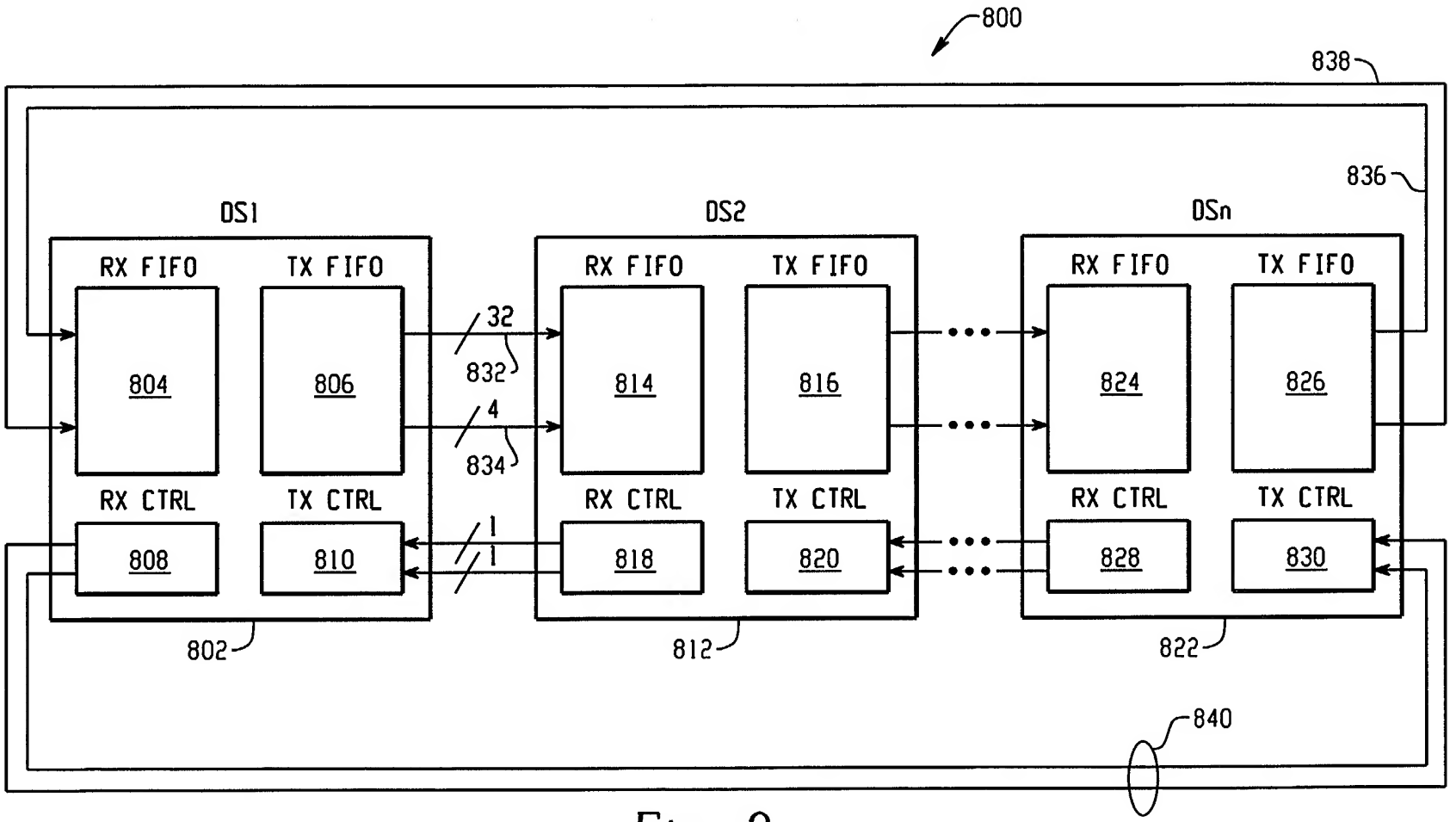
800
838
836
DS1
DS2
DSn
RX FIFO
TX FIFO
804
806
814
816
824
826
32
832
4
834
RX CTRL
TX CTRL
808
810
818
820
828
830
1
1
802
812
822
840

Fig. 8

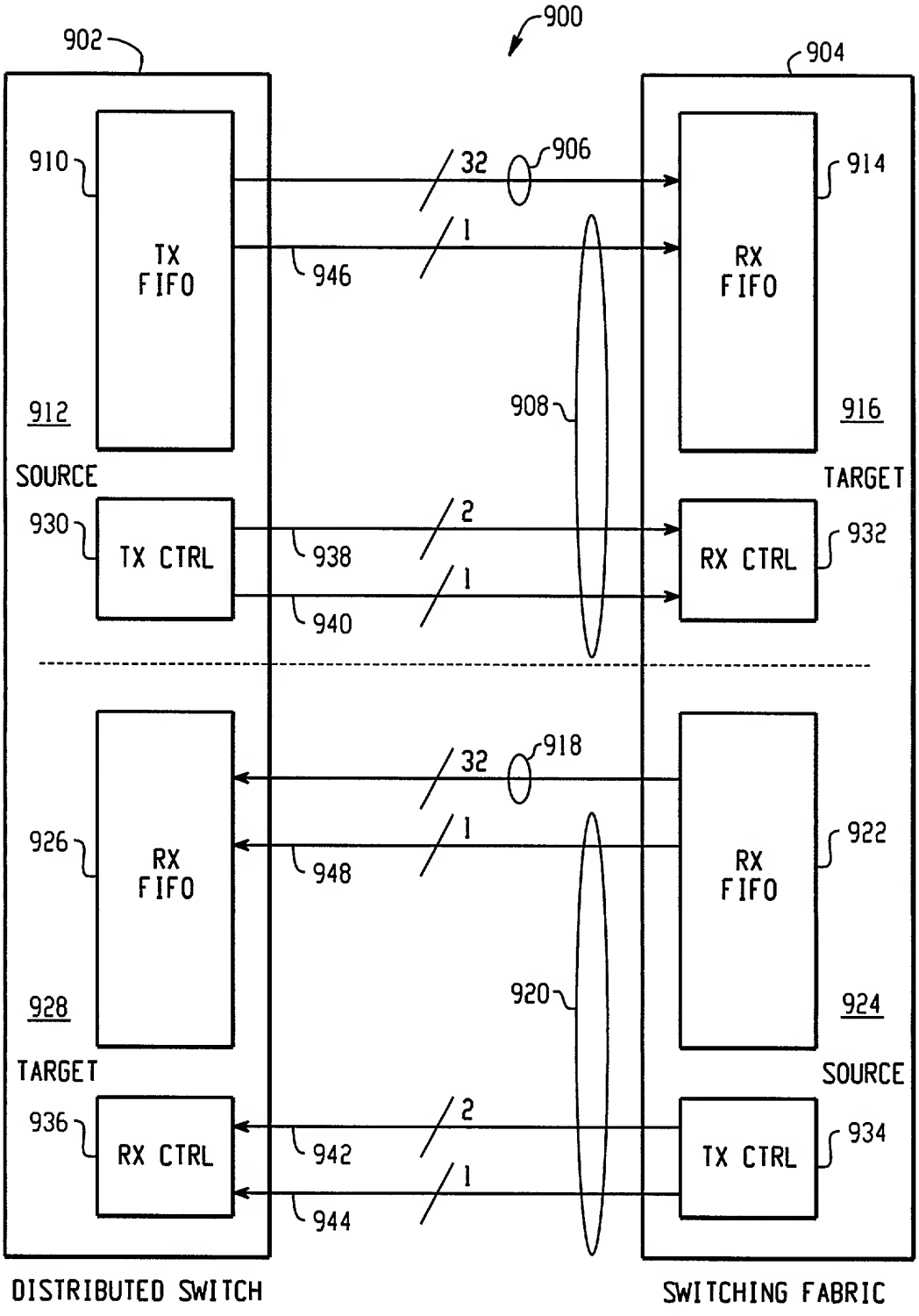
900
902
904
910
TX FIFO
912
SOURCE
32
906
1
946
908
914
RX FIFO
916
TARGET
930
TX CTRL
2
938
1
940
RX CTRL
932
926
RX FIFO
928
TARGET
32
918
1
948
920
922
RX FIFO
924
SOURCE
936
RX CTRL
2
942
1
944
TX CTRL
934
DISTRIBUTED SWITCH
SWITCHING FABRIC

Fig. 9

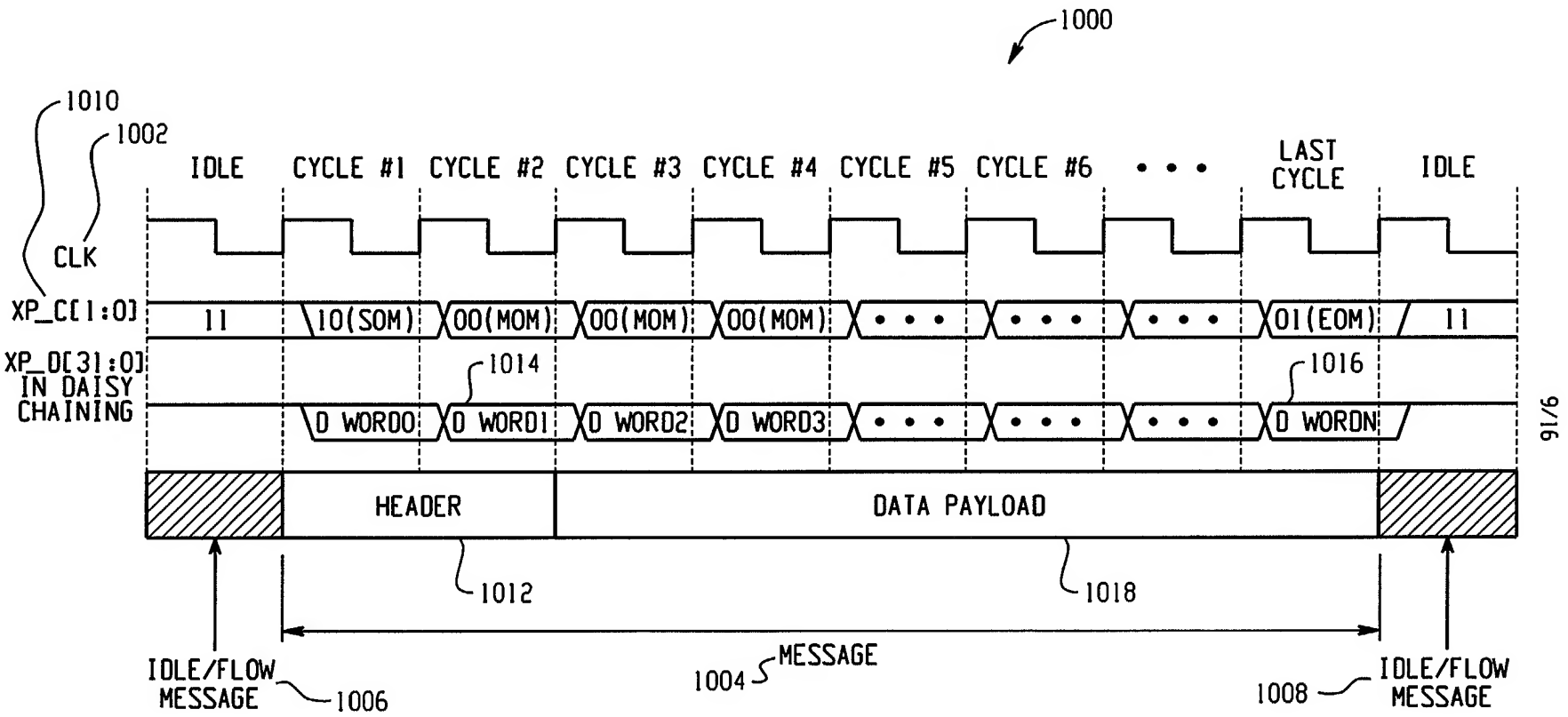
1000
1010
1002
IDLE
CYCLE #1
CYCLE #2
CYCLE #3
CYCLE #4
CYCLE #5
CYCLE #6
LAST CYCLE
IDLE
CLK
XP_C[1:0]
11
10(SOM)
00(MOM)
00(MOM)
00(MOM)
01(EOM)
11
XP_D[3:0] IN DAISY CHAINING
1014
1016
D WORD0
D WORD1
D WORD2
D WORD3
D WORDN
HEADER
DATA PAYLOAD
1012
1018
IDLE/FLOW MESSAGE
1006
1004
MESSAGE
1008
IDLE/FLOW MESSAGE

Fig. 10

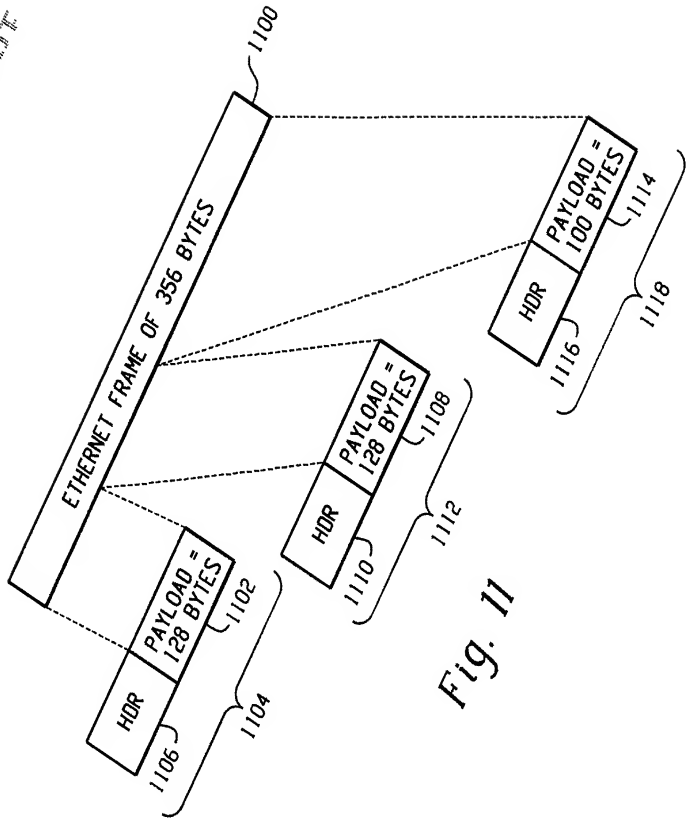
1100
ETHERNET FRAME OF 356 BYTES
PAYLOAD = 128 BYTES
1102
HDR
1106
1104
PAYLOAD = 128 BYTES
1108
HDR
1110
1112
PAYLOAD = 100 BYTES
1114
HDR
1116
1118

Fig. 11

UNICAST FRAME SCHEDULING REQUEST-FOUR WORDS (TYPE 000) 1200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		0		SOURCE DEV ID				SOURCE PORT ID				DEST PORT ID				R		DEST DEV ID					000			FRAME SIZE (UNIT=32 BYTES)						
	L3	VLAN ID (12 BITS)												TI	TO			XP	FRAME ID (RX BUFFER HANDLE) (12 BITS)													

Fig. 12a

LAN UNICAST FRAME DATA REQUEST-FOUR WORDS (TYPE 001, SUBTYPE=000000) 1210

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		0		SOURCE DEV ID				SOURCE PORT ID								R		DEST DEV ID					001			000000						
																						FRAME ID (RX BUFFER HANDLE) (12 BITS)										

Fig. 12b

LAN UNICAST FRAME DATA REJECT-FOUR WORDS (TYPE 001, SUBTYPE=100000)

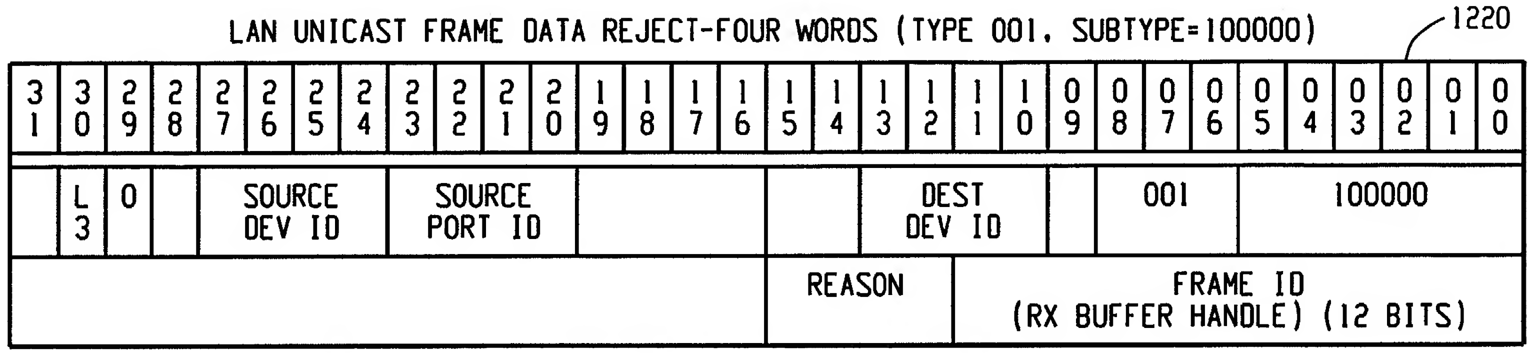

Fig. 12c

LAN UNICAST DATA TRANSFER-START OF FRAME(SOF)-FOUR WORDS (TYPE 110)

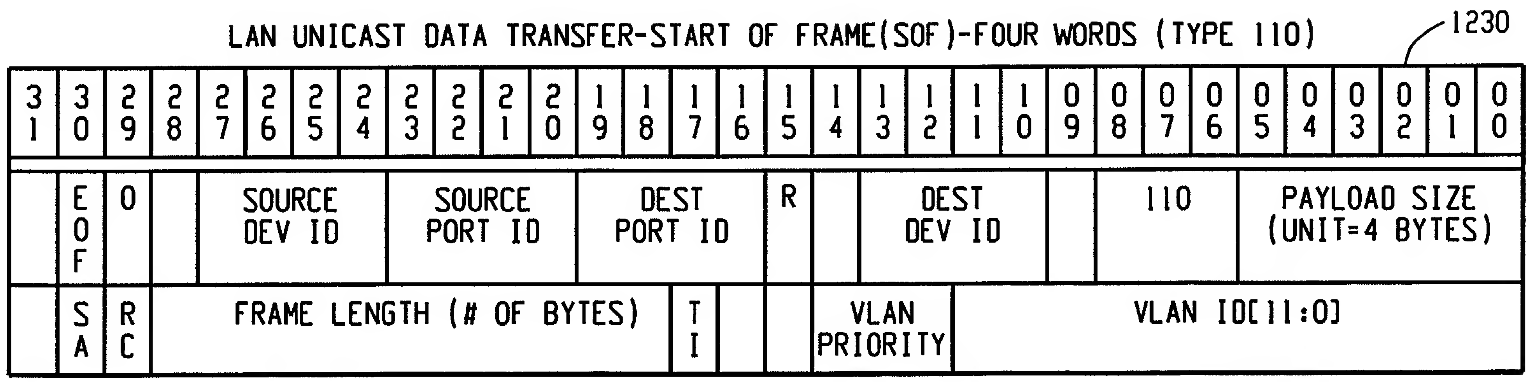

Fig. 12d

LAN UNICAST FRAME DATA TRANSFER-CONTINUOUS FRAME-TWO WORDS (TYPE 010) 1240

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	EOF	0		SOURCE DEVICE ID				SOURCE PORT ID				DEST PORT ID						DEST DEV ID					010			PAYLOAD SIZE (UNIT=4 BYTES)					

Fig. 12e

MULTICAST FRAME DATA TRANSFER-START OF FRAME (SOF)-FOUR WORDS (TYPE 111) 1250

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SA	EOF	HP	RC	SOURCE DEVICE ID				TOTAL FRAGMENT COUNT (UNIT=128 BYTE FRAGMENT)				LSB OF BYTE COUNT		FRAME SEQ.#		TI	XP		HASH KEY				111			PAYLOAD SIZE (UNIT=4 BYTES)					
MG	VLAN PRIORITY			VLAN ID/MULTICAST GROUP INDEX												DESTINATION DEV ID BIT MAP (16 BITS)															

Fig. 12f

MULTICAST FRAME DATA TRANSFER FOR CONTINUOUS FRAGMENT-TWO WORDS (TYPE 011) 1260

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	EOF	HP		SOURCE DEVICE ID				TOTAL FRAGMENT COUNT (UNIT= 128-BYTE FRAGMENT)				LSB OF BYTE COUNT		FRAME SEQ. #								011		PAYLOAD SIZE (UNIT=4 BYTES)							

Fig. 12g

FLOW CONTROL/IDLE MESSAGE-TWO WORDS (TYPE INDICATED BY XP_C[1:0]=00) 1270

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LINK STATUS (HIGH=LINK UP; LINK STATUS OF PORT 0 ON BIT 16, LINK STATUS OF PORT 1 ON BIT 17, AND SO ON)																						DF (DEVICE FLAVOR)		PORT NUMBER		UPDATE		ICHY	XOFF BITS		
																											HMC	LMC	DATAREQ	SCHREQ	UC

Fig. 12h

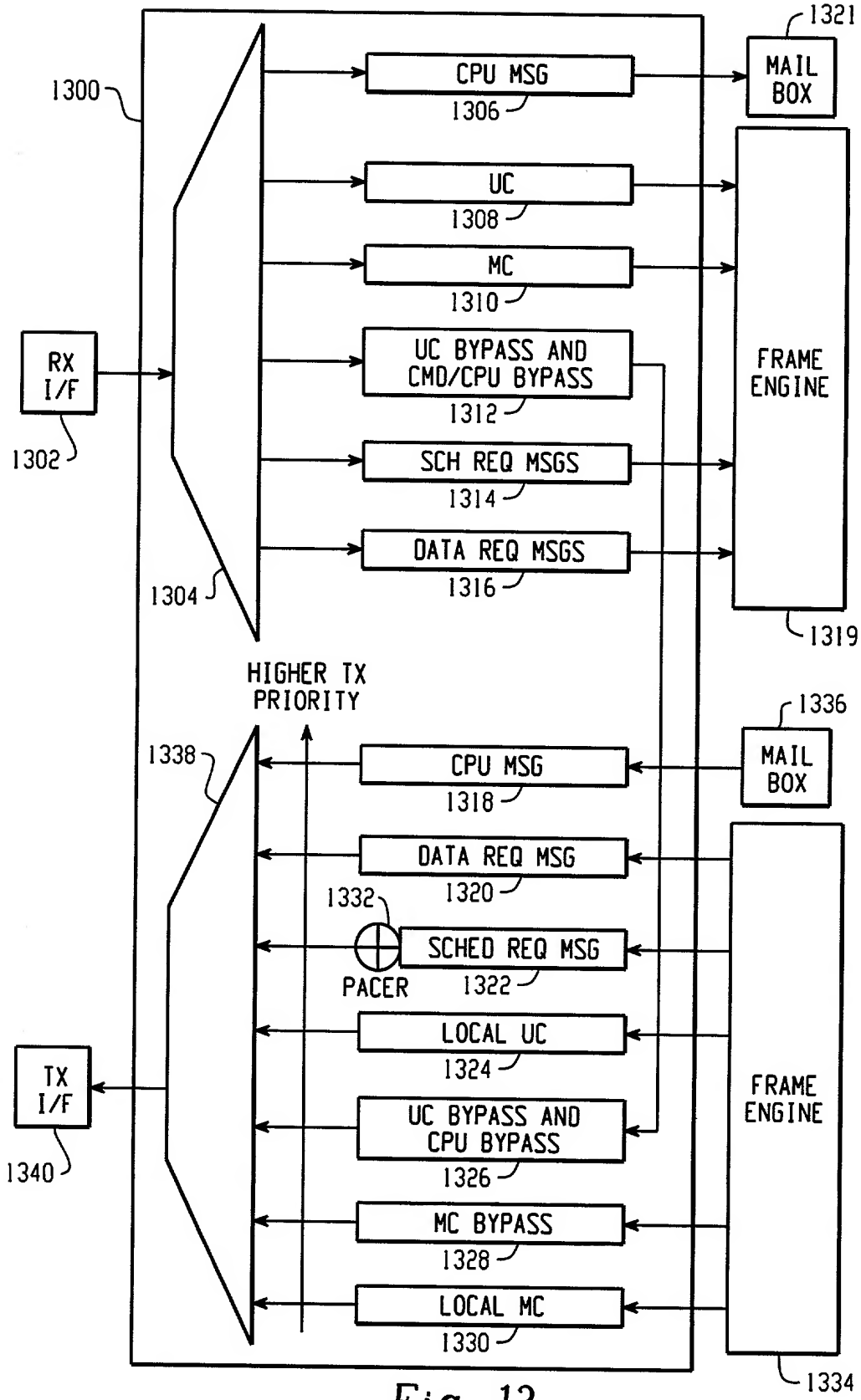
1321
MAIL BOX
1300
CPU MSG
1306
UC
1308
MC
1310
UC BYPASS AND CMD/CPU BYPASS
1312
SCH REQ MSGS
1314
DATA REQ MSGS
1316
FRAME ENGINE
1319
RX I/F
1302
1304
HIGHER TX PRIORITY
1336
MAIL BOX
1338
CPU MSG
1318
DATA REQ MSG
1320
1332
SCHED REQ MSG
1322
PACER
LOCAL UC
1324
UC BYPASS AND CPU BYPASS
1326
MC BYPASS
1328
LOCAL MC
1330
FRAME ENGINE
1334
TX I/F
1340

Fig. 13

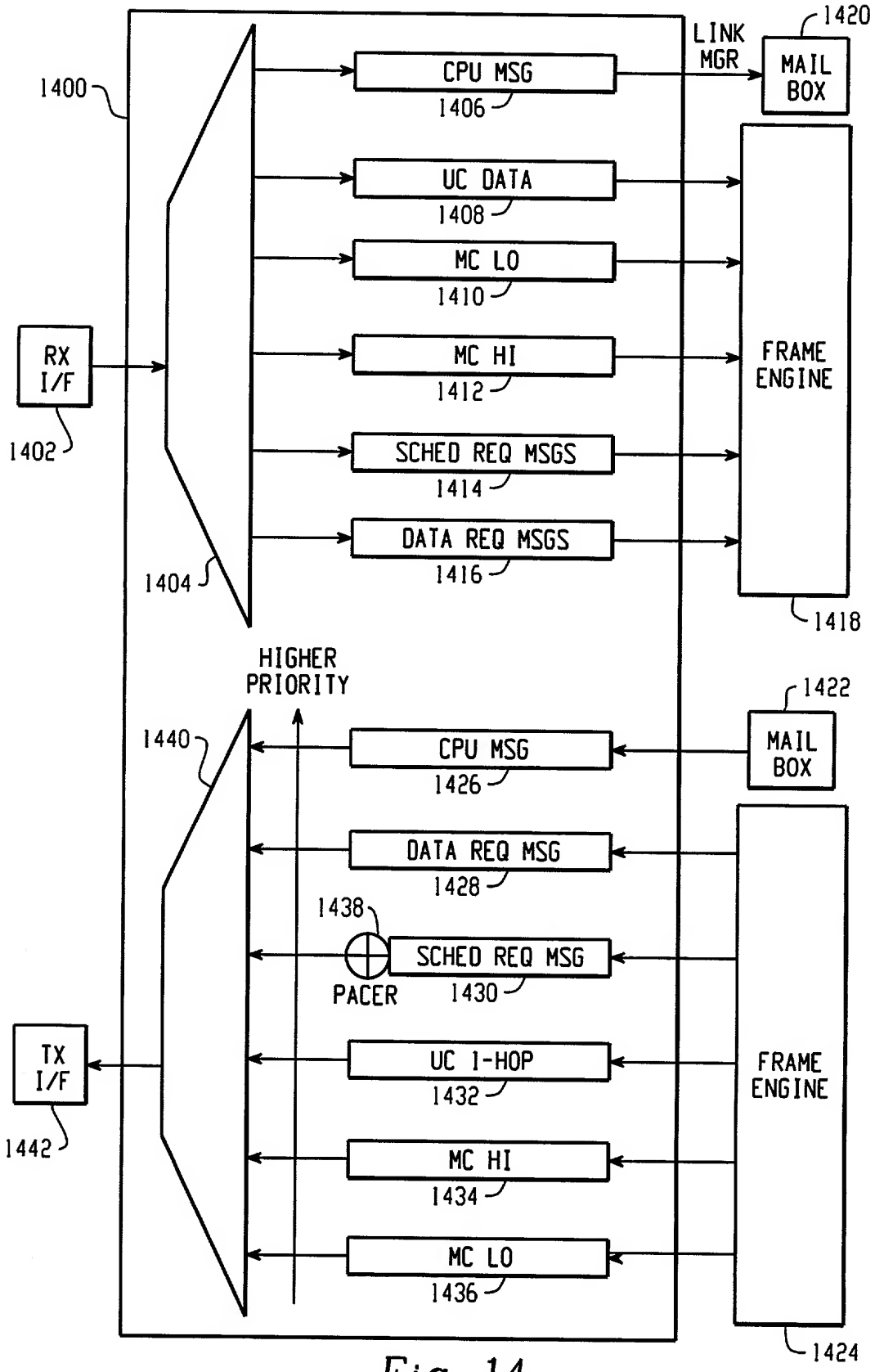
1400
RX I/F
1402
1404
CPU MSG
1406
UC DATA
1408
MC LO
1410
MC HI
1412
SCHED REQ MSGS
1414
DATA REQ MSGS
1416
LINK MGR
1420
MAIL BOX
FRAME ENGINE
1418
HIGHER PRIORITY
1440
CPU MSG
1426
DATA REQ MSG
1428
1438
SCHED REQ MSG
PACER
1430
UC 1-HOP
1432
MC HI
1434
MC LO
1436
TX I/F
1442
1422
MAIL BOX
FRAME ENGINE
1424

Fig. 14